Fast Response Validation of Storion Flow Battery Stacks for LDUPS™ Systems

Abstract

Storion Energy's vanadium redox flow battery (VRFB) stack power assembly, integrated within TerraFlow Energy's Long Duration Uninterruptible Power Supply (LDUPS™) architecture, delivers ultra-fast DC-link control for AI data centers and mission-critical infrastructure—while unlocking new grid service opportunities at scale.

Storion's VRFB stack power assembly is shown to deliver ultra-high output speeds, and function like a capacitor with the potential for hours of available energy. Integrating the Storion stack with TerraFlow Energy's unique LDUPS™ design enables sub-5 ms bidirectional current control that stabilizes load events and maintains continuous power quality across generator, grid, and inverter transitions. TerraFlow's integration of a VRFB directly into the DC bus architecture takes full advantage of Storion's stack microsecond-class electrochemical reaction speeds. The result of combining the two systems is a single long-duration system that enhances operational resilience, reduces generator stress, and enables fast-response ancillary services.

Key findings:

- **Stack Intrinsic speed:** Single-cell testing shows ≈8.1 µs reaction time and ≈43 A/µs slew (area-scaled), confirming the stack and chemistry are not the rate-limiting factor.
- **System response:** In UPS tests, the inverter output reaches its target current in ≈250 µs; stack takeover completes in ≈1.2–2.5 ms, depending on initial current.
- **Stability:** An 8.5 s / 14.3 kHz burst sequence showed no drift in current, voltage, or energy per cycle, confirming stable high-frequency behavior.

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1. Introduction

The electric grid is being rebuilt around inverter-based renewables, rapid electrification, and concentrated new loads—and the disturbance timescale has collapsed from minutes to milliseconds. Transient events such as cloud cover over utility-scale PV, gusts across wind fleets, EV charging pulses, semiconductor step loads, and synchronized accelerator bursts in AI data centers now create sharp, coordinated swings in real power. Meanwhile, the retirement of synchronous generation has reduced system inertia and governor-based damping, causing frequency and voltage deviations to develop faster and propagate farther. With interconnection queues and network upgrades often years out, simply adding capacity is no longer a timely or viable option.

The market is driving towards fast, local, bidirectional control, and the system must be capable of sourcing or absorbing energy on the same timescale as the disturbance. This class of control stabilizes operations internally while turning speed into value through emerging ancillary-service products.

Historically, facility power trains were designed around minutes-to-hours contingencies—double-conversion UPS systems for ride-through and generators for endurance. These remain essential for long-duration reliability but are fundamentally mismatched to 10–50 ms dynamics. The mechanical inertia of engines and turbines, along with governor and fuel-air constraints, pushes meaningful power adjustments into the hundreds of milliseconds or seconds. From a DC-link perspective, they are effectively one-quadrant devices—able to supply power but not absorb it during sudden load rejection—and are bound by minimum-load limits. At the same time, system operators are increasingly pricing speed: Fast Frequency Response (FFR), Very Fast Containment (VFAS), Dynamic Regulation, and other fast-response products all reward assets that can modulate active power within sub-second horizons.

This convergence of grid and facility dynamics demands a new architecture—one that operates on power-electronic timescales rather than mechanical ones.

LDUPS™ redefines the battery's role, not as standby backup, but as a central component of a continuous energy strategy. This dramatically changes the dynamics associated with the battery and shifts its requirements to achieve dynamic load support, extended energy delivery, along with seamless integration of distributed resources.

This paper presents evidence that Storion's flow battery stacks meet the stringent transient response and current-sharing requirements of LDUPS™ applications, validating their role in next-generation critical power systems.

2. LDUPS™ Architecture and System Integration

LDUPS™ employs a dual-conversion architecture (rectifier → DC link → inverter) with an optional tertiary inverter path for secondary output to grid or alternate load. This topology maintains

constant DC-link isolation between the grid and critical loads, ensuring uninterrupted power delivery even under severe transient conditions.

At the system's core, the flow battery connects directly across the DC link—functioning like a capacitor with hours of available energy. This configuration allows sub-10 ms bidirectional current transitions and enables seamless charge and discharge reversals in response to fast load dynamics.

Key operational capabilities include:

- Response time: <5 ms design target with demonstrated <3 ms reversal capability.
- Duration: 10+ hours of endurance for extended ride-through and load management.
- Bidirectional operation: Supports instantaneous load rejection and absorption.
- Load isolation: Continuously decouples sensitive loads from grid-side disturbances.
- Grid and generator coordination: Enables slower and more controlled ramping, reducing stress and operational risk.
- ISO controllability: Converts large, variable loads into grid-responsive resources capable of providing PFR/FFR and dynamic regulation.

By pairing fast electrochemical response with long-duration energy storage, LDUPS™ offers both operational resilience and revenue potential—supporting data centers, utilities, and industrial facilities seeking stable, flexible, and market-participating power architectures.

3. Stack Based Electrochemical Background and Translation to Time-Domain Behavior

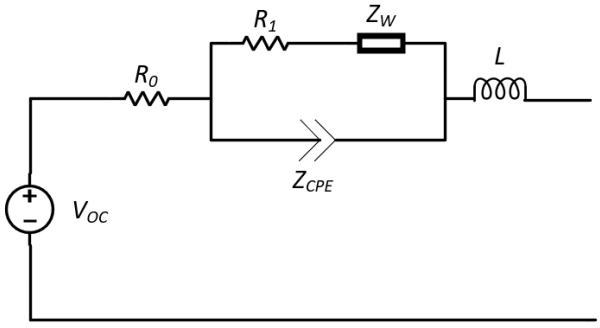

Figure 3-1. Equivalent circuit model for a battery stack

This section establishes the electrochemical framing used throughout this work and connects that framing to the time-domain behavior of the flow battery stack and chemistry that matters for LDUPS™ operation. We rely on electrochemical analysis and supporting EIS data gathered within our development program, which fit the stack to a standard small-signal model consisting of an ohmic term R_o, a charge-transfer branch expressed as R_t in parallel with a constant-phase element (CPE), a diffusion contribution of Warburg form, and a small series inductance (see Figure 3-1).

The parameters were normalized per cell and per active-area unit, allowing direct and transparent scaling from laboratory coupons to multi-cell stacks without altering the underlying chemistry assumptions.

Section 3.a applies these normalized parameters to two concrete geometries that bracket the configurations used later in this work: a single lab-scale cell and a ten-cell stack with cell geometry identical to that of our production stack. Table 3-1 summarizes the internal model parameters expressed per-unit area and per cell count, showing how the ohmic, interfacial, and diffusive elements scale across configurations. Absolute values are obtained from the normalized impedances by the geometric relations in Equation 3-1 through Equation 3-3.

$$R_{abs} = R_{norm} \cdot N / A$$

Equation 3-1. Geometry scaling for resistance.

$$L_{abs} = L_{norm} \cdot N / A$$

Equation 3-2. Geometry scaling for inductance.

$$Q_{abs} = Q_{norm} \cdot A / N$$

Equation 3-3. Geometry scaling for CPE magnitude.

Section 3.b then translates this impedance model into time-domain bounds relevant to LDUPS™ control. Together, these results bound what we should expect to see in subsequent tests: At short times, the current slew is set by available voltage headroom and the loop inductance of the DC path (Equation 3-4). At millisecond scales, the takeover follows an RC time constant (Equation 3-5). The stack's internal inductance is too small to limit the early ramp, and its kinetic corner is already faster than the LDUPS™ target window, so the chemistry does not impose a fundamental barrier to a sub-5 ms response.

$$dI/dt \approx V_{headroom} / L_{loop}$$

Equation 3-4. Loop-inductive current ramp (early window).

$$\tau \approx C_{psu} \cdot R_{eff}$$

Equation 3-5. Late-window takeover time constant.

Table 3-1. Internal EIS-Derived Model Parameters (normalized)

Parameter	Expression / Value
R_o [Ω·cm²]	0.26
R_1 [Ω·cm²]	0.01
Z_W [Ω·cm²]	6.26×10^{-2} / √(jω)
Z_CPE [Ω·cm²]	1 / [3.82×10^{-2}·(jω)^0.97]
Z_L [Ω·cm²]	2.64×10^{-6}·jω

(All entries represent Storion internal data normalized per active area; absolute values follow from geometry scaling as described in text.)

a. What EIS analysis shows and how it scales

Storion's electrochemical impedance analysis provides representative parameters for Storion stacks under practical operating conditions. Table 3-1 fits the measured spectra to a standard series model that consists of an ohmic term R0, a charge-transfer branch captured by R1 in parallel with a near-capacitive constant-phase element (CPE), a diffusion term with semi-infinite Warburg form, and a small series inductance. The values in Table 3-1 are normalized per cell and per unit area in Ω·cm². This normalization is important because it lets us scale cleanly from a single laboratory cell to multicell stacks by multiplying by the number of series cells and dividing by the active area per cell.

For clarity, we restate the Table 3-1 normalized parameters used below: R0 = 0.26 Ω·cm², R1 = 0.01 Ω·cm², CPE with Q = 0.0382 S·s^α·cm^{-2} and α ≈ 0.97, Warburg coefficient σ = 0.0626 Ω cm² $s^{-1/2}$, and series inductance L = 2.64×10^{-6} H·cm². Absolute values follow the rules established in Equation 3-1 through Equation 3-3, where N is the series cell count, and A is the per-cell active area in cm².

Table 3-2 and Table 3-3 present the translated impedance parameters for the lab-scale and 10-cell commercial stacks, respectively. Because α is close to unity, the constant-phase element (CPE) behaves nearly as a true capacitor. For clarity, we also report an effective mid-band capacitance, shown in Equation 3-6, to provide a practical sense of scale in farads.

$$C_{eff} \approx 0.038 \cdot A / N$$

Equation 3-6. Effective mid-band capacitance for near-ideal CPE.

Table 3-2. EIS parameters scaled to a single sub-scale cell.

Quantity	From Table 1 (normalized)	Scaled value (absolute)
Ohmic resistance R0	0.26 Ω·cm²	10.4 mΩ
Charge-transfer resistance R1	0.01 Ω·cm²	0.40 mΩ
Series inductance L	2.64×10^{-6} H·cm²	106 nH
CPE parameter Q, α	0.0382, 0.97	0.955 S·s^α, 0.97
Effective capacitance C_eff	—	0.95 F
Warburg coefficient σ	0.0626 Ω·cm²·s^−1/2	2.50×10^{-3} Ω·s^1/2

Table 3-3. EIS parameters scaled to a 10-cell stack.

Quantity	From Table 3-1 (normalized)	Scaled value (absolute)
Ohmic resistance R0	0.26 Ω·cm²	3.25 mΩ
Charge-transfer resistance R1	0.01 Ω·cm²	0.125 mΩ
Series inductance L	2.64×10^{-6} H·cm²	33 nH
CPE parameter Q, α	0.0382, 0.97	3.056 S·s^α, 0.97
Effective capacitance C_eff	—	3.04 F
Warburg coefficient σ	0.0626 Ω·cm²·s^−1/2	7.83×10^{-4} Ω·s^1/2

Two general conclusions follow from these numbers. First, the ohmic and charge-transfer contributions remain in the milliohm range for the 10-cell stack, which supports high instantaneous current for typical DC-bus headroom. Second, the internal series inductance scales to the tens of nanohenry range for the 10-cell configuration, which is much smaller than inductance introduced by cabinet cabling and bus structures. As a result, internal stack inductance is not expected to set the early current ramp in time-domain tests. The CPE's near-ideal behavior indicates that the double layer can accept or supply charge quickly over the mid-frequency band, while the Warburg term governs diffusion primarily at low frequency.

b. Using EIS to bound transient behavior and confirm sub-5 ms viability

Electrochemical impedance provides the chemical bandwidth and resistive floor that translate directly into time-domain bounds. The charge-transfer branch defines a kinetic corner through the product of R1 and the interfacial capacitance associated with the CPE. Using the Table 3-1 normalized values, Equation 3-7 gives $\tau_ct \approx (0.01\ \Omega\cdot cm^2) \times (0.038\ F\cdot cm^{-2}) \approx 0.38$ ms. This time constant is effectively invariant with series cell count and plate area for a stack of identical cells because R1 scales with N/A while the interfacial capacitance scales with A/N; the product remains the same. In other words, the reaction kinetics captured by EIS are already in the sub-millisecond regime at small signal.

$$\tau_ct \approx R_1 \cdot C_dl$$

Equation 3-7. Charge-transfer kinetic time constant.

Diffusion appears in EIS as a Warburg element (Equation 3-8) whose magnitude falls as 1/√f. A convenient way to judge its relevance is to compare the Warburg magnitude with R1; with the Table 3-1 parameters, the diffusion-to-kinetic crossover lies at low frequency. That crossover is well below the frequencies associated with sub-millisecond electrical steps, so diffusion is not expected to control the initial current response when bus voltage is perturbed. It will contribute at longer scales that are outside the critical LDUPS™ transfer window.

$$Z_W = \sigma / \sqrt{(j\omega)}$$

Equation 3-8. Semi-infinite Warburg diffusion impedance.

These EIS results inform the electrical design model directly. In the short-time regime, the current ramp is primarily set by the available voltage headroom and the loop inductance of the DC path, while the stack's internal inductance from Table 3-1 is negligible compared with external hardware. In the millisecond regime, the dominant shape of the takeover follows the product of the bus capacitance and the effective series resistance seen by that capacitor. The stack contributes a small part of that resistance through R0 + R1 in the milliohm range; the remainder lies in interconnects, joints, diodes, and buswork. Because the chemistry corner is already faster than a few milliseconds and the stack's resistive floor is low, there is no fundamental chemical limitation preventing a sub-5 ms response. The implication is clear: if the electrical path to and from the stack is dimensioned with low loop inductance and low effective series resistance, the stack chemistry supports the reaction speed that LDUPS™ requires. The next sections present time-domain tests that validate this conclusion with measured data.

4. Experimental Platforms and Instrumentation

a. Single-Cell

The single-cell apparatus, shown in Figure 4-1, isolates the intrinsic electrochemical speed of the Storion architecture. A sub-scale cell is conditioned to 1.5 V and then connected to a 0.1 Ω non-inductive resistor via a mechanical switch. Mechanical actuation eliminates solid-state turn-on artifacts, enabling accurate microsecond-class measurements. A companion test replacing the cell with a capacitor verified that fixture risetime is not limited by stray wiring or bandwidth. Instantaneous cell voltage and current are recorded to compute slew rate and 0 to 100% response times.

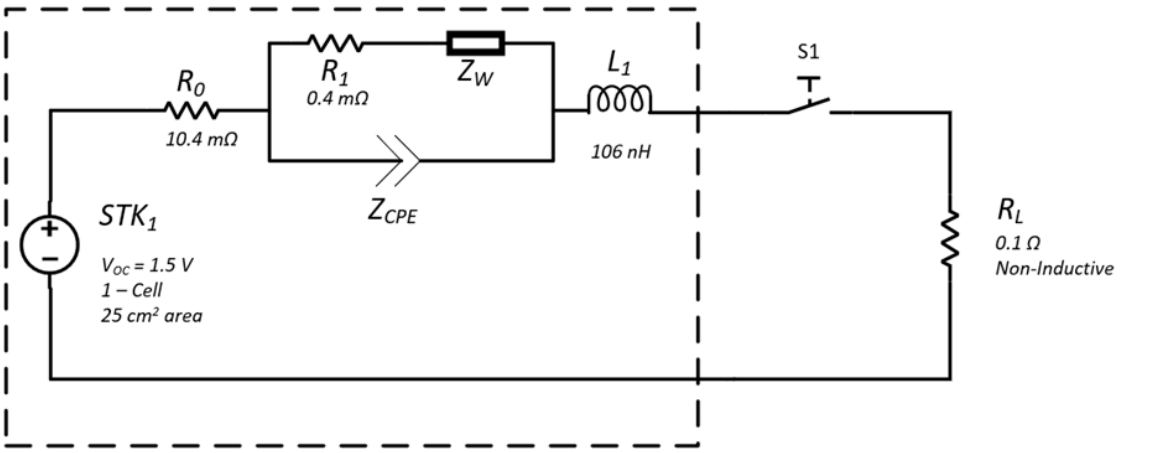

Figure 4-1. Single-cell transient response apparatus. The sub-scale Storion cell is switched into a 0.1 Ω non-inductive load using a mechanical switch to avoid SSR turn-on artifacts.

b. UPS

The UPS-level platform reproduces system parasitics encountered in practice. As shown in Figure 4-2, a laboratory rectifier (16.4 V, 200 A limit) supplies the DC bus through a series protection diode. The inverter is emulated by a programmable electronic load commanded for 25 A/µs slew. A ten-cell Storion stack connects to the bus via remote cabling; measured parasitics and elements are summarized in Table 4-1. Instrumentation captures I_psu, I_stack, I_load, the capacitor contribution via KCL, and node voltages at the PSU, load, and stack terminals. This arrangement allows us to visualize early-window inductive ramps, bus droop and ringing, and late-window exponential takeover.

The influence of initial stack current on takeover dynamics was evaluated under three operating regimes: Charge → Discharge (CH → DSCH), Float → Discharge (FLT → DSCH), and Discharge → Discharge (DSCH → DSCH). The outcomes are summarized in Table 4-2. In all cases, the inverter achieved its commanded output within ≈ 250 µs. At the millisecond scale, the subsequent takeover adheres to the RC-governed time constant given by Equation 3-5, with component values listed in Table 4-1.

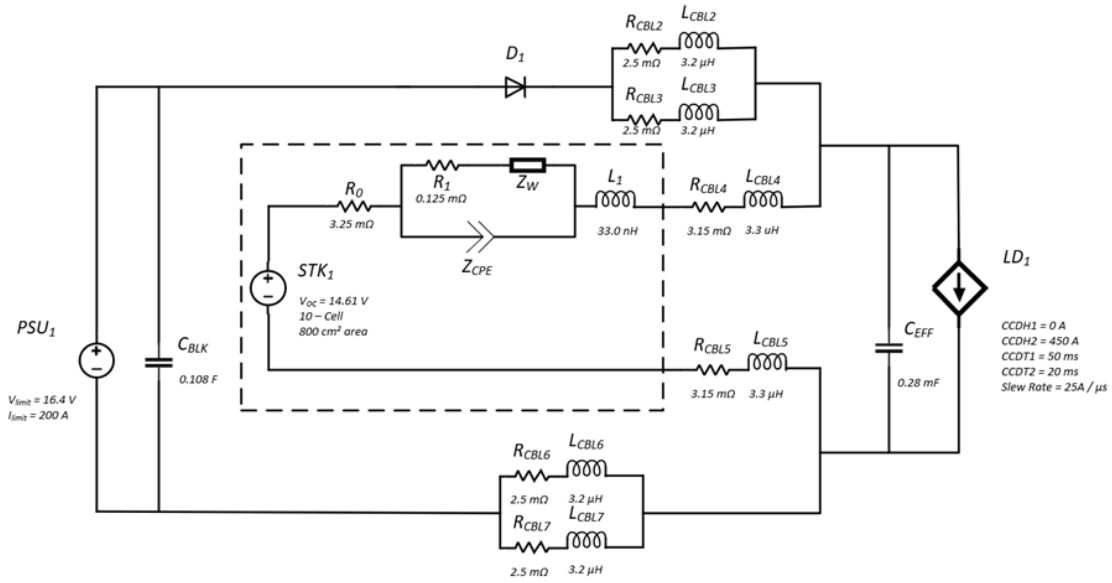

Figure 4-2. UPS-level DC-bus test configuration. Includes 16.4 V/200 A rectifier with series diode, realistic cabling, and segregated bulk (0.108 F) and load-bus (≈0.28 mF) capacitances.

Table 4-1. Electrical parameters of the UPS test platform.

Path / Element	Resistance (per lead)	Inductance (per lead)	Loop Total
PSU → Load	1.25 mΩ	1.6 µH	2.5 mΩ / 3.2 µH
Stack → Bus	3.15 mΩ	3.3 µH	6.3 mΩ / 6.6 µH
Bulk capacitance	—	—	0.108 F
Load-bus capacitance	—	—	≈0.28 mF

Table 4-2. Initial-condition regimes and observed takeover behavior.

Regime	Load Step (A)	Rectifier Behavior	Stack Current Transition	Stack Takeover Time	Notes
CH→DSCH	0 → 450	≈110 → 200 A in ≈110 µs	−110 → +250 A	≈2.5 ms	Worst-case reversal (charge→discharge)
FLT→DSCH	200 → 450	Held at 200 A	0 → +250 A	≈1.2 ms	Float start
DSCH→DSCH	300 → 450	Held at 200 A	+100 → +250 A	≈1.2 ms	Continuing discharge

5. Results: Single-Cell Transient Capability

To assess the intrinsic electrochemical speed of a Storion single cell, actuation limits were removed, and a hard mechanical switch was employed. The initial 7.5 µs pre-bounce interval of the resulting step response is shown in Figure 5-1. Within this 0–7.5 µs window, the cell exhibits a rapid current rise; beyond approximately 7.5 µs, mechanical contact bounce distorts the waveform. Consequently, all quantitative metrics are derived from the pre-bounce region, yielding a 7.5 µs total response, an initial slew rate of 3.6 A/µs, a secondary slew of 0.61 A/µs, and an overall average of 1.33 A/µs.

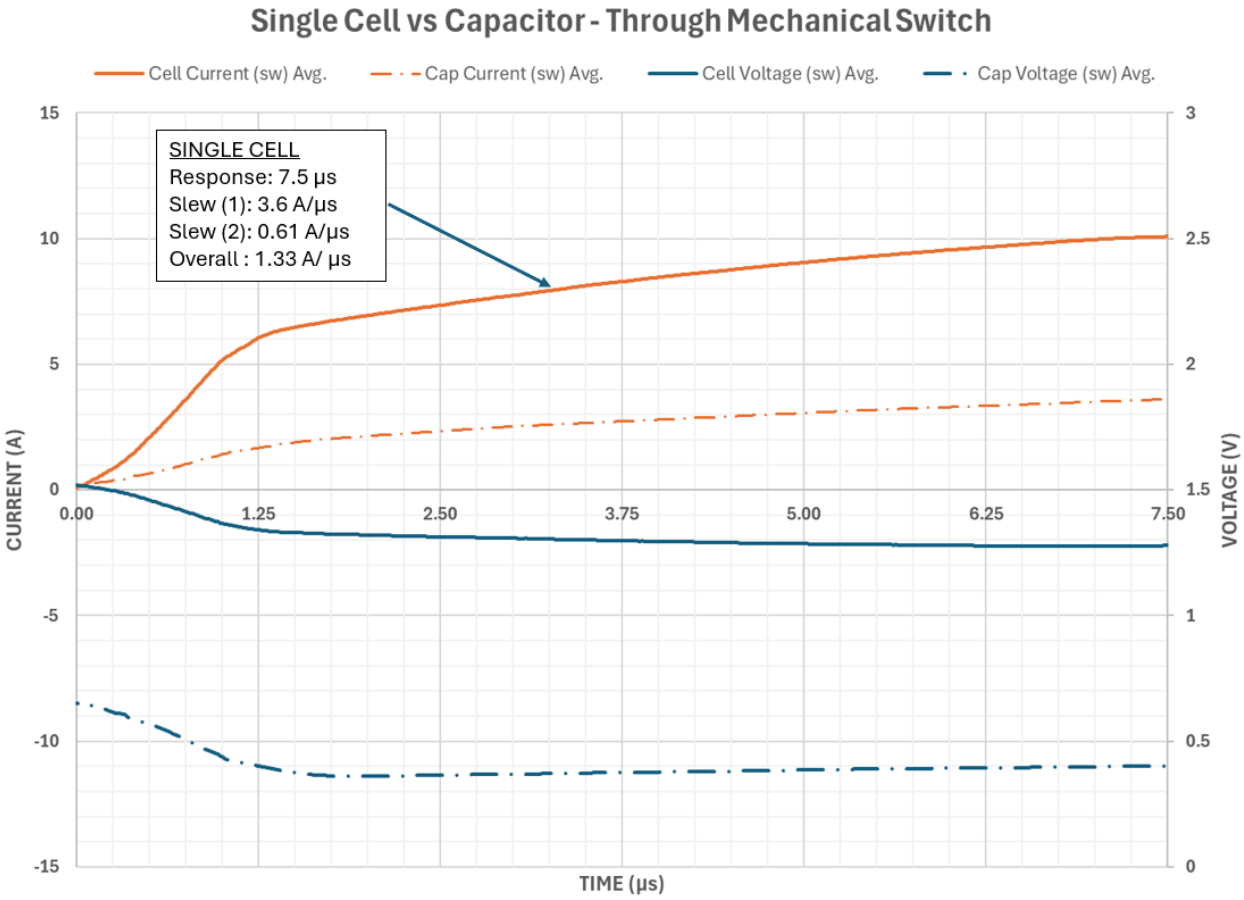

Figure 5-1. Single-cell step via mechanical switch with capacitor surrogate overlay. Interpretation is limited to the first 7.5 µs due to contact bounce.

The capacitor trace in Figure 5-1 acts as a control that proves the fixture is not the limiting factor. Because the capacitor has no electrochemical dynamics, it follows the ideal wiring/instrument response; any overshoot or slope changes with the cell therefore arise from the cell rather than fixture bandwidth or parasitics.

Figure 5-2 compares the actuation methods. The solid-state relay (SSR) produces a cleaner, lower-distortion waveform, though its turn-on is slightly rate-limited, appearing as a slower apparent rise consistent with its switching characteristics. In contrast, the mechanical switch introduces contact-bounce spikes and ripples beyond roughly 7.5 µs, which is why all quantitative metrics are taken from the pre-bounce interval. The key procedural insight is that, in microsecond-scale measurements, the actuation method can dominate the observed response. When a solid-state element is used, its switching behavior must be characterized and de-embedded; otherwise, the cell chemistry may be incorrectly blamed for artifacts introduced by the actuator. Conversely, when a mechanical switch is used, any contact bounce must be excluded from interpretation.

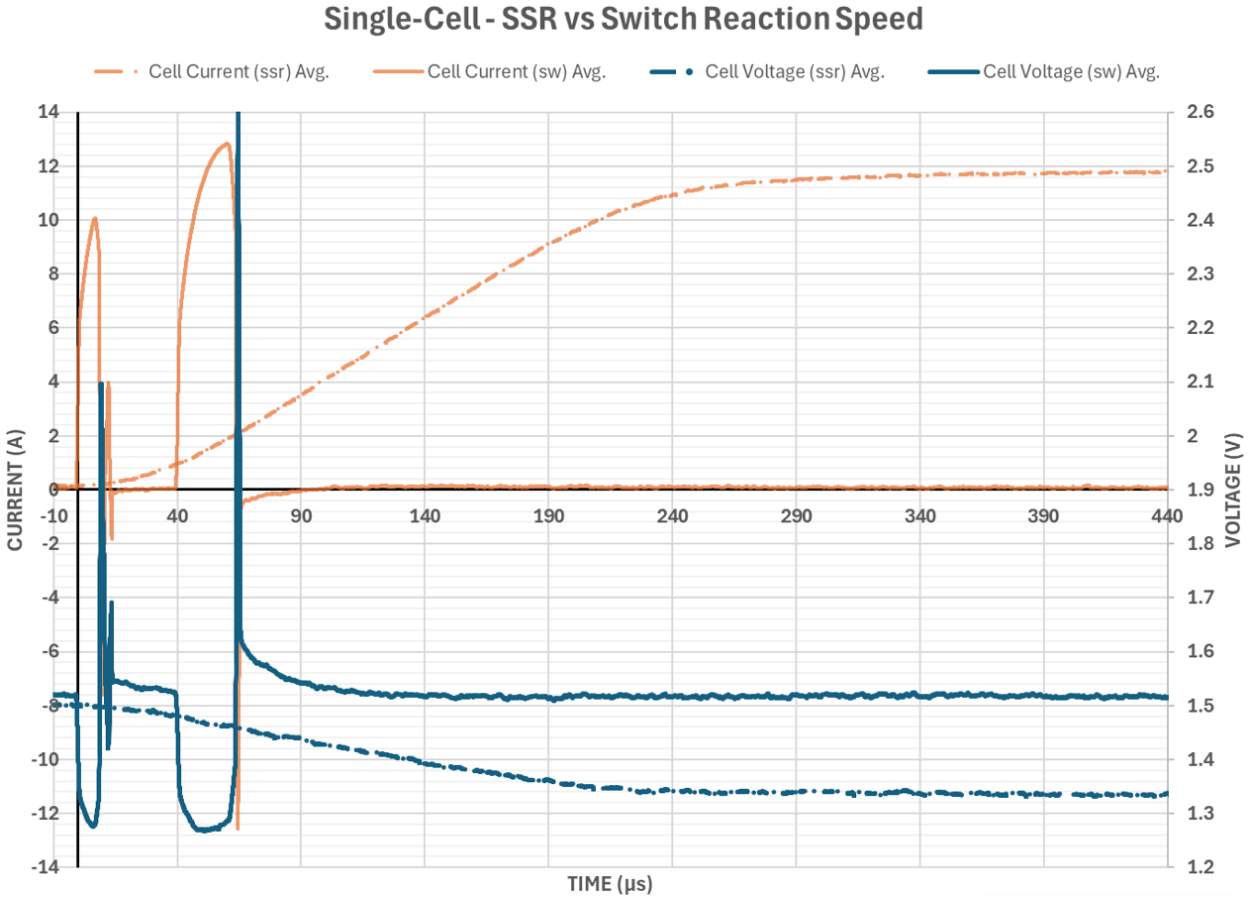

Figure 5-2. SSR versus mechanical-switch actuation of the same single cell. The SSR yields the cleaner, lower-distortion waveform; the mechanical switch shows contact-bounce spikes that complicate interpretation beyond ~7.5 µs.

Interpreting these results after area-scaling from the sub-scale cell to the production-scale stack provides useful perspective. The ≈8.1 µs rise indicates that the combined ohmic and double-layer elements readily support the required current when referenced to the 1.5 V headroom. Any markedly slower response would have pointed to limitations in charge-transfer kinetics or mass transport, yet neither is evident on these timescales. Equally important, the ≈43 A/µs figure

demonstrates that the cell can source or sink charge at rates far exceeding the demands of a millisecond-scale UPS. For a 10-cell design, this microsecond-class behavior persists, with current slew scaling directly with active area; practical limits therefore shift to wiring, capacitance, and control rather than chemistry. In short, the cell is not a liability—it is an asset whose intrinsic speed allows system designers to balance capacitance, interconnect parasitics, and bandwidth without encountering a hard electrochemical limit.

Table 5-1. Summary of Single-Cell Transient Performance

Configuration	Reaction Time (0 to 100%) [µs]	Max Slew Rate [A/µs]
Single Sub-Scale Cell	8.1	1.33
10-Cell Stack (Scaled)	8.1	43

6. Results: UPS-Level Transients and the Role of Initial Conditions

Having established that the cell chemistry itself is capable of microsecond-class response, the next question is how that intrinsic speed manifests when the cell is embedded within the full DC-bus environment of a UPS. At this level, the stack no longer operates in isolation but interacts with the rectifier, diode, cabling, and capacitor network — the same coupled elements that shape transient behavior in any double-conversion UPS — that together define the electrical boundary conditions. The goal of this section is to trace how those external elements shape the apparent response time and to quantify the relative contributions of inductance, resistance, and capacitance under realistic operating regimes. Using the same instrumentation and scaling as in Section 3, we examine the composite behavior of the stack, rectifier, and load during representative current steps.

Figure 6-1 overlays a Stack-Only transient with a Float→Discharge (FLT→DSCH) UPS transient to isolate electrical-pathway effects from intrinsic stack kinetics. In the initial ≈100 µs interval, the two traces are essentially coincident: the current rise follows the loop-inductive ramp governed by interconnect inductance and available bus headroom rather than electrochemical rate limits. This relationship is expressed by Equation 6-1, which describes the instantaneous slope of current rise.

$$dI/dt \approx V_headroom / L_loop$$

Equation 6-1. Loop-inductive ramp during initial interval.

Beyond this common inductive segment, the trajectories diverge. In the Stack-Only case, no parallel energy reservoir exists, so the response remains a single-slope inductive ramp until steady-state. In the UPS case, once the inverter output reaches its setpoint, the bulk DC-link capacitor sources the instantaneous deficit between commanded load and the sum of rectifier and stack currents. The system then transitions to the late-window evolution characterized by the RC-governed time constant shown in Equation 6-2 — a universal DC-link behavior independent of battery chemistry. The load behavior follows Kirchhoff's Current Law, summarized in Equation 6-3.

When I_cap ≈ 0 in the Stack-Only case, I_load ≈ I_stack; with I_cap > 0 in the UPS run, the load is met immediately while the stack current continues to climb along the RC-governed path.

$$\tau \approx C_psu \cdot R_eff$$

Equation 6-2. Capacitor-to-stack handoff time constant.

$$I_load = I_psu + I_stack + I_cap$$

Equation 6-3. KCL at the DC bus.

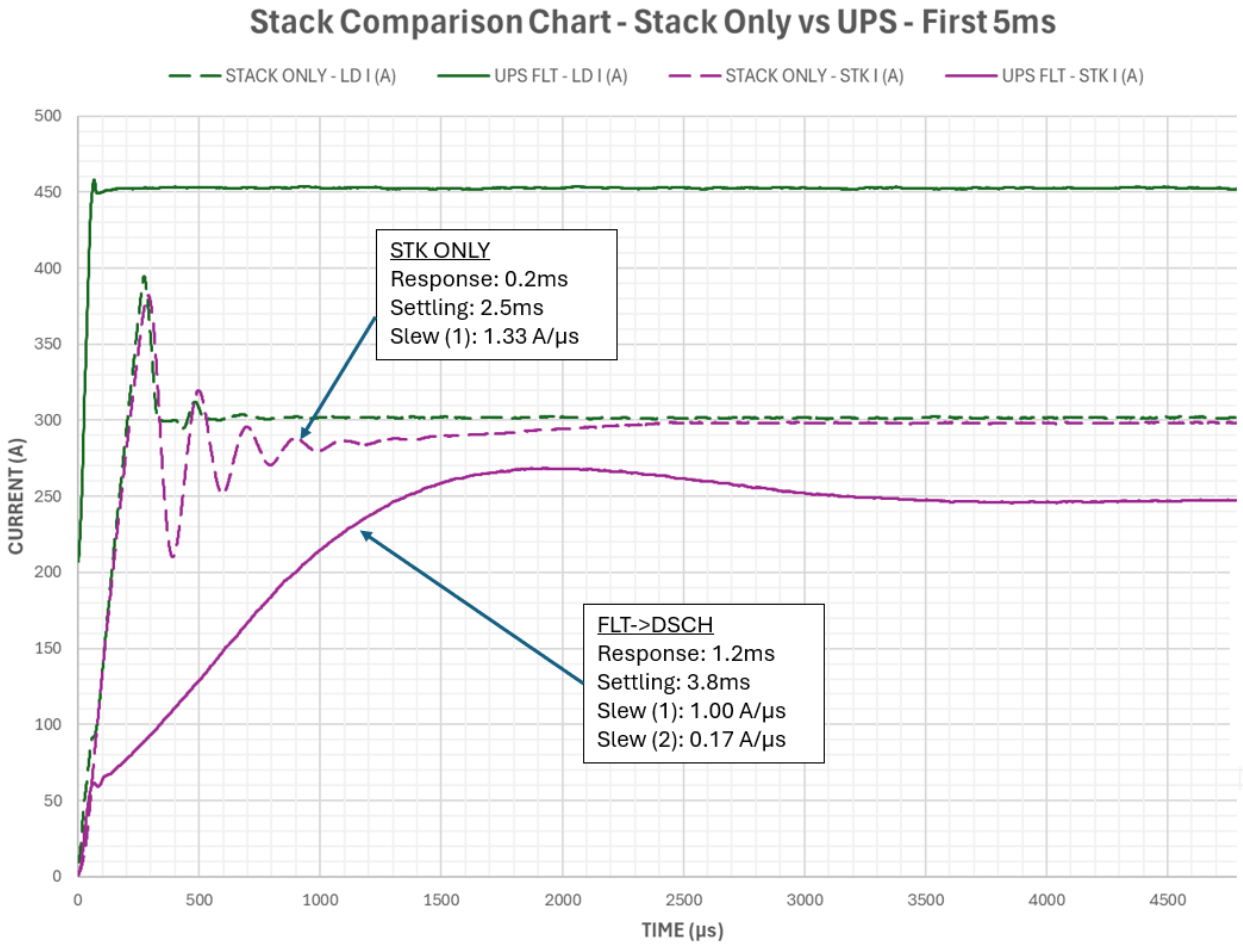

Figure 6-1. UPS-level transient comparison showing Stack-Only (dashed) and CH→DSCH (solid) cases. The Stack-Only trace exhibits interconnect-limited behavior (≈1.33 A/µs, 0.2 ms rise, 2.5 ms settling), while the FLT→DSCH trace illustrates full UPS dynamics.

Measured values are consistent with this interpretation. The Stack-Only trace exhibits an early-window slew of ≈1.3 A/µs with a 0–100 % traversal of ≈241 µs, whereas the UPS FLT→DSCH run reaches the inverter command in ≈250 µs but requires ≈1.2 ms for the capacitor-to-stack handoff

to complete, in line with the installed C_psu and observed R_eff. The ≈30× gap between the Stack-Only slew and the area-scaled single-cell capability (≈43 A/µs for an equivalent 10-cell geometry) identifies external loop inductance and usable voltage headroom—not interfacial kinetics or mass transport—as the limiting factors in the early window.

Operationally, Figure 6-1 shows identical terminal behavior until the capacitor engages; beyond that point, timing is an architectural outcome set by C_psu and R_eff. Customer-visible output remains sub-millisecond, while stack takeover proceeds on the millisecond scale. Improving either interval is an electrical design exercise: reduce L_loop and increase practical headroom to steepen the inductive rise; reduce R_eff and judiciously size and locate C_psu to shorten the RC handoff. The chemistry is not rate-limiting within the UPS transient window.

Table 6-1. UPS-level transients under different initial conditions (corresponding to Figure 6-1, Figure 3-1, and Figure 6-2).

Case	Starting Condition	Load Step (A)	Stack Current Transition (A)	0–100 % Response	Settling Time	Early-Window Slew (A/µs)	Late-Window Slew (A/µs)	Interpretation
Stack-Only	Isolated stack path	—	0 → +100	≈ 241 µs	≈ 2.5 ms	≈ 1.33	—	Inductive single-slope; interconnect sets rate
CH → DSCH	Charging → Discharging	0 → 450	−110 → +250	≈ 2.5 ms	≈ 7.0 ms	≈ 1.18	≈ 0.11	Two-slope: inductive early ramp then τ ≈ C·R
FLT → DSCH	Floating → Discharging	200 → 450	0 → +250	≈ 1.2 ms	≈ 3.8 ms	≈ 1.00	≈ 0.17	Faster takeover—no reversal required
DSCH → DSCH	Discharging → Discharging	300 → 450	+100 → +250	≈ 1.2 ms	≈ 3.7 ms	≈ 0.58	≈ 0.10	Smallest deficit; quickest response

Note: Takeover times reflect DC-link C_psu and R_eff along the installed path. This is a general UPS design dependency and is not specific to LDUPS™ or to the Storion stack.

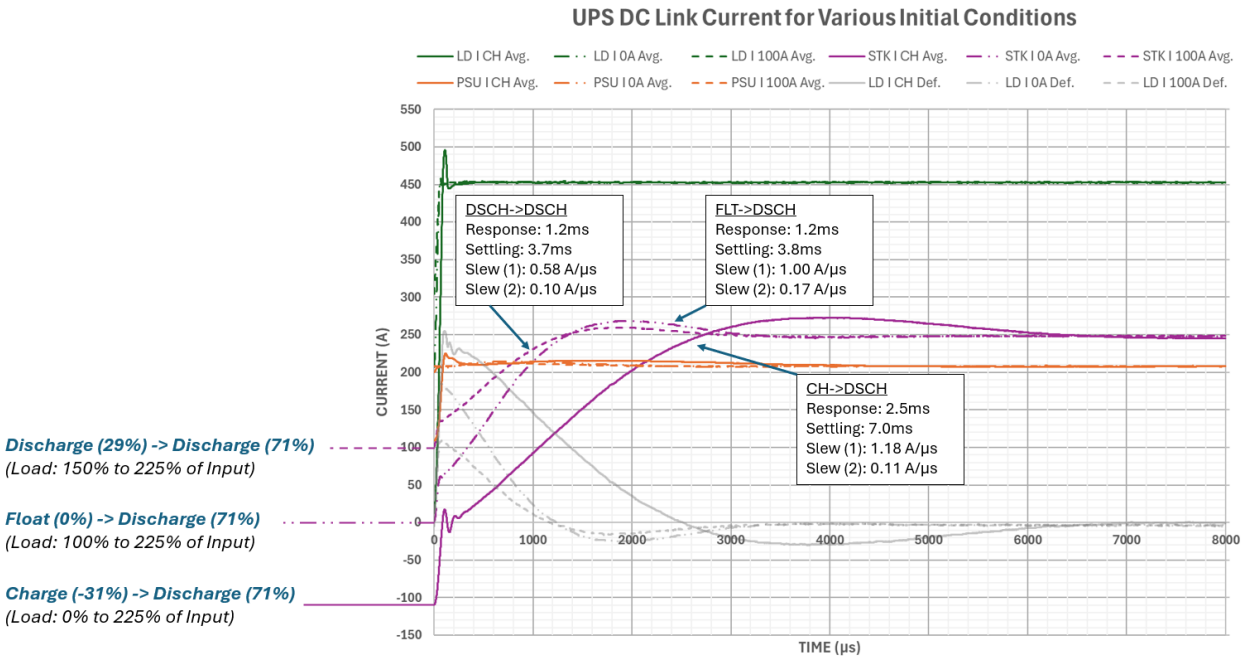

Figure 6-2. Comparison of UPS transients for three initial-condition regimes. The inverter output reaches its target within ≈250 µs in all cases, while stack takeover depends on starting current: ≈2.5 ms for CH→DSCH, ≈1.2 ms for FLT→DSCH, and ≈1.2 ms for DSCH→DSCH

Figure 6-2 and Table 6-1 generalize this observation by comparing three initial-condition regimes. In CH→DSCH the inverter load steps from 0 A to 450 A. The rectifier rises from ≈110 A to its 200 A limit over ≈110 µs, and the stack transitions from −110 A to +250 A over ≈2.5 ms. In FLT→DSCH, the load steps from 200 A to 450 A while the rectifier is already at 200 A. At the same time, the stack climbs from 0 A to +250 A in ≈1.2 ms. In DSCH→DSCH, the load steps from 300 A to 450 A with the rectifier steady at 200 A; the stack moves from +100 A to +250 A also in ≈1.2 ms. Two features are striking. First, in every case the inverter output current reaches its commanded level within ≈250 µs, signaling that the customer-visible response is sub-millisecond even when the stack is still assuming its share. Second, the stack takeover time is tightly correlated with the starting current such that whenever the stack begins at or above 0 A, the takeover is ≈1.2 ms; when it begins in charge (negative current), the takeover roughly doubles to ≈2.5 ms.

This behavior can be fully understood through Kirchhoff's Current Law and the C–R framework. During the late window, the capacitor supplies the shortfall between I_load and I_psu and I_stack. The rate at which I_cap decays to zero is governed by how quickly the stack can increase its current along the available electrical path (Equation 6-2). When the stack begins in the positive operating quadrant (0 A or higher), current reversal is unnecessary and the deficit to be covered is smaller, producing a τ-like rise that resolves in approximately 1.2 ms for the present interconnect. By contrast, a discharge initiated from a charging condition entails a larger directional and magnitude excursion, requiring the capacitor to carry the deficit for longer. The resulting ≈ 2.5 ms takeover

under otherwise identical hardware still yields sub-millisecond UPS output deviation, easily meeting the overall LDUPS™ response target of < 5 ms.

It is worth emphasizing that the commanded inverter slew (25 A/µs) is not achieved in any test because bus dynamics and control interactions inherently limit the realized slew. This outcome does not reflect a shortcoming of the stack but rather illustrates that the inverter, rectifier, and DC-bus interconnect operate as a coupled system whose limits must be co-engineered — as is standard practice for any UPS aiming for sub-5 ms DC-link control. From an application standpoint, what matters is that the inverter reaches its commanded output rapidly and without excessive droop or ringing, while the battery assumes its share quickly enough to prevent bulk-capacitor depletion or overheating. The data confirms both conditions are satisfied. Moreover, the parameters that further shorten takeover are purely electrical—lower loop inductance in the first 250 µs, reduced effective resistance thereafter, and judicious capacitance sizing.

7. Sustained Bursting and Stability

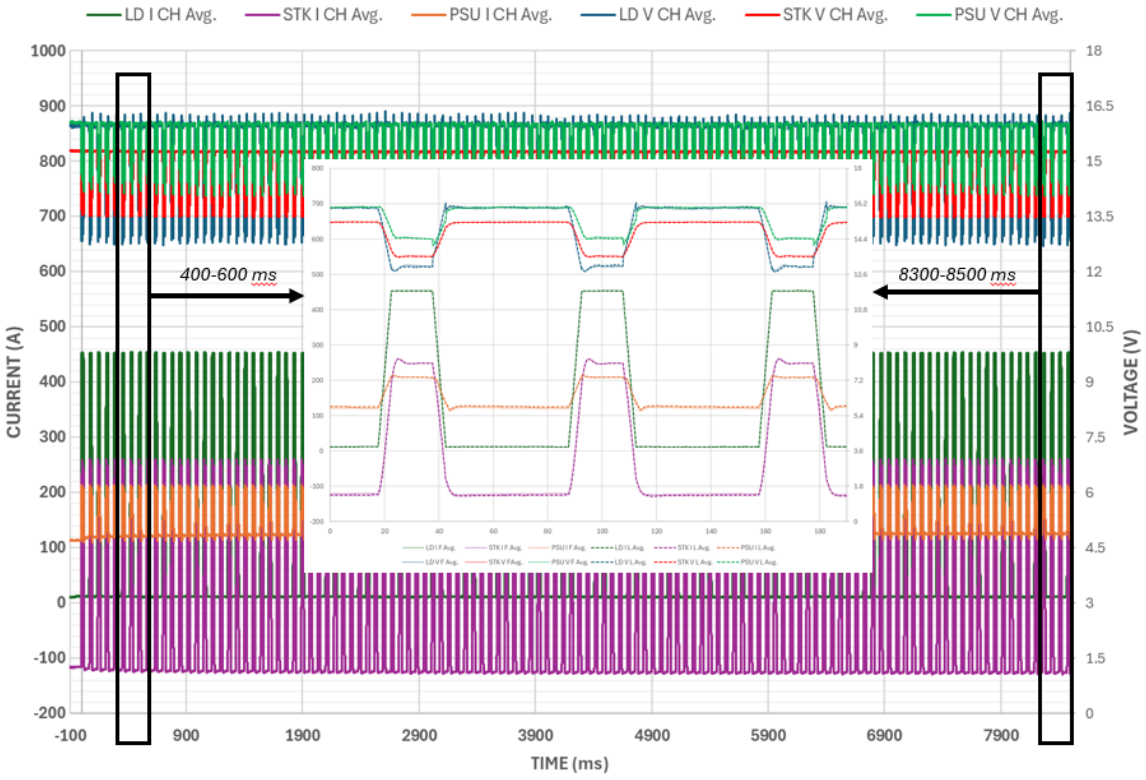

Figure 7-1. UPS-level sustained burst test at 14.3 kHz for 8.5 s showing stable current and voltage behavior across all channels. The inset compares early-run (400–600 ms) and late-run (8300–8500 ms) windows, demonstrating negligible drift in amplitude, phase, or energy per cycle. Load, stack, and PSU traces remain consistent in both magnitude and timing, confirming dynamic stability of the flow-battery stack under repeated high-frequency transient operation.

To test whether rapid transients accumulate into drift or performance fade, we executed an 8.5 second burst sequence at 14.3 kHz with approximately 30% duty cycle. This profile mimics the on-off computational rhythm of AI inference loads and stresses both the electrical and electrochemical subsystems. We compared three representative cycles early in the run with three late in the run. Within measurement resolution, the waveforms are indistinguishable in amplitude, timing, and energy transfer per cycle (≈0.4 mAh/cycle; ≈48.4 mAh total over the full sequence). The stack charge voltage shows only a small shift possibly attributable to ohmic heating and minor state-of-charge movement, neither of which alters the transient character.

The absence of drift matters for two reasons. First, it indicates that the electrochemical system remains inside a linear-like operating envelope for the duration of the burst, such that neither mass-transport nor thermal limits are approached on these timescales. Second, it validates the co-design assumption that the capacitor handles the ultrafast energy exchange while the stack provides the millisecond energy handoff, without either element being asked to do both jobs simultaneously. For data-center operators this translates to consistent UPS behavior across bursts, which is essential for maintaining voltage quality upstream of sensitive IT loads.

8. Design Guidance for Sub-5 ms LDUPS™ with Storion Stacks

At the system level, the parameters that ultimately shape transient behavior are architectural rather than chemical. While the Storion stack itself can respond in microseconds, the surrounding DC-bus network determines how that intrinsic speed appears at the terminals. Designers therefore consider a range of electrical factors that influence the overall waveform of a transient event—chief among them the extent of DC-bus voltage droop, the degree and damping of DC-bus ringing, and the time it takes for the stack to assume its steady-state current.

These outcomes depend on how the physical and electrical layout of the system is executed. Bus geometry, conductor spacing, and cabinet arrangement define the distributed inductance and parasitic capacitance that govern the initial voltage motion during a current step. High inductance deepens the first voltage dip and lengthens oscillations, while compact and symmetric layouts yield faster recovery. The effective resistance seen by the bus—including cable, joint, and protection-device losses—sets the damping of those oscillations and the slope of voltage recovery. Lower resistance typically reduces droop magnitude and energy loss, but must be weighed against thermal, safety, and cost constraints.

Capacitor sizing and distribution further influence how the bus maintains voltage between the instant of a load step and the point where the stack current fully compensates. Larger bulk capacitance can moderate the droop but extend the time required to recharge, whereas smaller distributed capacitors can localize the transient and improve damping. The optimal configuration depends on application priorities such as allowable bus-voltage deviation, transient repetition rate, and thermal limits.

In short, achieving sub-5 ms performance is an exercise in managing the DC-bus environment rather than altering the chemistry. By shaping bus impedance, minimizing resistive losses, and staging capacitance thoughtfully, designers can ensure that the Storion stack's intrinsic electrochemical speed translates into stable, predictable, and repeatable system-level behavior.

In practice, these findings translate directly to commercial LDUPS™ systems, where optimized DC-bus design allows Storion's intrinsic electrochemical speed to deliver consistent, sub-5 ms performance in full-scale TerraFlow Energy deployments.

9. Conclusions

Storion stack power assemblies for vanadium flow batteries meet the dynamic response needs of long-duration UPS applications. Single-cell testing, translated to stack scale, demonstrates a no-load-to-full-load reaction time of ≈8.1 µs and a maximum current slew rate of ≈43 A/µs. Complementary tests on a ten-cell stack, operated in a "stack-only" configuration without the rest of the UPS hardware, confirm that this microsecond-class behavior persists at practical scale: the stack achieved a 0–100% current transition in roughly 241 microseconds and was only limited by external wiring inductance and fixture geometry rather than by chemistry. Both results sit far below the millisecond response window required for LDUPS™ operation, collectively proving that the Storion architecture is fundamentally fast enough to support sub-5 ms system performance.

In real-world LDUPS™ deployments, overall transient performance depends on proper system design. The DC bus transient is managed first by the DC-link capacitor bank, which supplies or absorbs the immediate surge, while the flow-battery stack provides the sustained power that follows. Appropriate cabling geometry, minimized loop inductance, low effective series resistance, and right-sized capacitor banks ensure that the UPS output responds within specification and that the stack assumes load smoothly and reliably.

Together, the results confirm that integration of the Storion VRFB stack within the LDUPS™ architecture enables the platform to achieve the fast-response and long-duration performance required for grid-scale applications.

In short: the chemistry is fast enough; achieving consistent sub-5-millisecond UPS output is a matter of sound DC-bus architecture.

Appendix A. Glossary of Variables, Abbreviations, and Technical Terms

This appendix provides concise definitions and explanations of the physical quantities, electrical laws, and electrochemical parameters referenced throughout this paper.

A1. Units and Metric Prefixes

All quantities in this report use SI (International System) units. The table below summarizes the most common base units and prefixes.

Symbol	Meaning	Multiplier
A	Ampere (unit of current)	—
V	Volt (potential difference)	—
Ω	Ohm (unit of resistance)	—
H	Henry (unit of inductance)	—
F	Farad (unit of capacitance)	—
J	Joule (unit of energy)	—
W	Watt (unit of power)	—
C	Coulomb (unit of charge)	—
s	Second (time)	—
m	milli	$\times 10^{-3}$
µ	micro	$\times 10^{-6}$
k	kilo	$\times 10^{3}$
M	mega	$\times 10^{6}$

A2. Symbols and Abbreviations Used in Formulas

Symbol	Definition
Q	Electric charge (coulombs)
C	Capacitance (farads) or Coulomb (unit of charge)—context clarifies
I	Current (in amperes)
R	Resistance (in ohms)
L	Inductance (in henries)
t	Time (in seconds)
E	Energy (in joules)
P	Power (in watts)

A3. Governing Laws and Time Constants

Ohm's Law: Defines the relationship between voltage, current, and resistance: V = I × R.

Kirchhoff's Current Law (KCL): The sum of all currents entering and leaving a node equals zero (e.g., I_load = I_psu + I_stack + I_cap).

Inductive ramp relation: Current slew rate in an inductive path is dI/dt = V/L.

Time constant (τ): Characteristic time for exponential change in RC or RL networks. For a capacitor, τ = R × C.

Voltage headroom: Available voltage margin between the supply (e.g., PSU output or stack OCV) and the instantaneous bus voltage across an inductor (e.g., the wires). It represents the effective voltage margin that can drive current change (dI/dt ≈ V/L) and determines how rapidly that current can change. A larger headroom enables a faster current ramp.

A4. Geometry-Scaled and Derived Parameters

Term	Definition
R_norm	Area-specific resistance (Ω·cm²) from EIS
R_abs	Absolute resistance scaled by area and cell count: R_abs = R_norm × N/A
L_norm	Area-specific inductance (H·cm²) from EIS
L_abs	Absolute inductance scaled by area and cell count: L_abs = L_norm × N/A
Q_norm	Area-specific CPE magnitude (F/cm²) from EIS
Q_abs	Absolute CPE magnitude scaled by area and cell count: Q_abs = Q_norm × A/N
C_eff	Effective capacitance from the CPE: C_eff = (Q × R^(1−α))^(1/α)

A5. Electrochemical Kinetic Terms

Term	**Definition**
t_ct	Charge-transfer time constant t_ct = R_1 × C_dl
R_1	Charge-transfer resistance (reaction-rate limitation)
C_dl	Double-layer capacitance at the electrode interface
Q, α	Constant-phase element parameters (α ≈ 1 implies near-ideal capacitance)
jω	Imaginary frequency variable in impedance models
N	Number of cells in series (e.g., 10 in stack). Used for scaling EIS parameters.
A	Electrode active area per cell (cm^2
R_0	Ohmic/contact resistance term of EIS model
σ	Warburg (diffusion) coefficient for semi-infinite diffusion impedance
τ	Time constant
Z_L	Inductive impedance jωL
Z_CPE	Constant-phase element impedance, modeling interfacial capacitance
Z_W	Warburg diffusion impedance (1/√f behavior)
Constant-phase element (CPE)	Non-ideal capacitor element with α exponent < 1
Double-layer capacitance	Electrochemical interfacial charge storage; represented by CPE
Warburg diffusion	Mass-transport impedance scaling as 1/√f
Charge-transfer kinetics	Finite reaction-rate limitation represented by R1 branch

A6. UPS Circuit Terms

Term	**Definition**
I_psu	Rectifier/Power-supply current feeding the DC bus
I_stack	Storion Energy stack current (positive = discharge, negative = charge)
I_load	Load/inverter current drawn from the DC bus
C_psu	Power-supply bulk/DC-link capacitance
R_eff	Effective series resistance seen by C_psu and stack
Early Window	Initial inductive phase limited by loop inductance and voltage headroom
Late Window	Capacitive phase governed by $\tau \approx C \times R$
Rectifier / Power-Supply (PSU)	A programmable DC source feeding the DC-link (DC bus) through a series diode that limits backfeed
Inverter / Load	A programmable DC sink that emulates inverter demand on the DC-link (DC bus). Programmed with a 25 A/us slew rate.
Slew Rate	Rate of current change (A/µs)
Settling Time	Time until steady-state current or voltage achieved after load step
Ringing	Transient oscillation of DC bus voltage or current after load step
CH->DSCH	Charge-to-discharge regime transition (negative to positive stack current)
FLT→DSCH	Float-to-discharge regime transition (near-zero to positive stack current)
DSCH→DSCH	Discharge-to-discharge regime transition (positive to more positive stack current)
Takeover Time	Time for stack current to fully replace DC bus bulk capacitor current
OCV	Open-circuit voltage of stack or cell
SSR	Solid-state relay, used in single cell switching tests
UPS	Uninterruptible Power Supply
VRFB	Vanadium Redox Flow Battery
DSCH	Discharge regime of stack (positive current)
CH	Charge regime of stack (negative current)
FLT	Float regime of stack (zero current)